CLAIMS

What is claimed is:

1. A method of fabricating a MOS transistor, the method comprising:

creating a form structure above a starting structure, the form structure having an opening exposing a single portion of the starting structure;

forming a semiconductor material in the opening of the form structure to create a formed semiconductor body having a single generally planar bottom surface above the starting structure, the formed semiconductor body comprising a first body portion, a second body portion, and a third body portion, the second body portion being disposed between the first and third body portions and having first and second sides and a top;

removing the form structure;

forming a gate structure disposed along at least a portion of the top and sides of the second body portion, the gate structure comprising a conductive gate electrode and a gate dielectric disposed between the gate electrode and the second body portion; and

doping the first and third body portions to form source/drains in the first and third body portions.

2. The method of claim 1, wherein forming the semiconductor material in the opening of the form structure comprises:

depositing the semiconductor material over the form structure and in the opening of the form structure; and

planarizing the semiconductor material to expose the form structure.

3. The method of claim 2, wherein the starting structure comprises a semiconductor and wherein depositing the semiconductor material comprises depositing epitaxial silicon, epitaxial silicon germanium, epitaxial germanium, or

epitaxial gallium arsenide over the form structure and in the opening of the form structure.

4. The method of claim 2, wherein depositing the semiconductor material comprises depositing epitaxial silicon over the form structure and in the opening of the form structure.

5. The method of claim 2, wherein the form structure comprises silicon nitride.

6. The method of claim 1, forming the semiconductor material in the opening of the form structure comprises forming silicon, silicon germanium, germanium, or gallium arsenide in the opening of the form structure.

7. The method of claim 1, wherein forming the semiconductor material comprises forming silicon in the opening of the form structure.

8. The method of claim 1, wherein the form structure comprises silicon nitride.

9. The method of claim 1, wherein creating the form structure comprises:

depositing a form layer material above the starting structure; and

selectively removing portions of the form layer material to create the opening exposing the single portion of the starting structure.

10. The method of claim 1, wherein forming the gate structure comprises:

forming a gate dielectric material over the formed semiconductor body;

forming a conductive gate electrode material above the gate dielectric material; and

selectively removing the gate electrode material over the first and third body portions of the formed semiconductor body to define a gate structure disposed along at least a portion of the top and sides of the second body portion.

11. A transistor, comprising:

a formed semiconductor body having a single generally planar bottom surface and being deposited over a starting structure, the formed semiconductor body comprising a first body portion, a second body portion, and a third body portion, the second body portion being disposed between the first and third body portions and having first and second sides and a top, the first and third body portions individually comprising doped source/drains; and

a gate structure disposed along at least a portion of the top and sides of the second body portion, the gate structure comprising a conductive gate electrode and a gate dielectric disposed between the gate electrode and the second body portion.

12. The transistor of claim 11, wherein the first, second, and third body portions are disposed along an axis, the axis being generally parallel to a plane of the wafer.

13. The transistor of claim 11, wherein the starting structure comprises a semiconductor and wherein the formed semiconductor body comprises epitaxial silicon, epitaxial silicon germanium, epitaxial germanium, or epitaxial gallium arsenide.

14. The transistor of claim 11, wherein the formed semiconductor body comprises epitaxial silicon.

15. The transistor of claim 11, wherein the formed semiconductor body comprises silicon, silicon germanium, germanium, or gallium arsenide.

16. The transistor of claim 11, wherein the second body portion comprises a channel having a channel length a channel width and a channel depth, and wherein the channel length, the channel width and the channel depth are generally equal.

17. The transistor of claim 16, wherein the channel length is about 25 nm or less.

18. The transistor of claim 11, wherein the second body portion comprises a channel having a channel length of about 25 nm or less.

19. A transistor, comprising:

a formed semiconductor body formed in an opening of a temporary form structure over a starting structure, the formed semiconductor body comprising a first body portion, a second body portion, and a third body portion, the second body portion overlying the starting structure between the first and third body portions and having first and second sides and a top, the first and third body portions individually comprising doped source/drains; and

a gate structure disposed along at least a portion of one or more of the top and sides of the second body portion, the gate structure comprising a conductive gate electrode and a gate dielectric disposed between the gate electrode and the second body portion.

20. The transistor of claim 19, wherein the first, second, and third body portions are disposed in a first plane generally parallel to a plane of the starting structure.

21. The transistor of claim 19, wherein the formed semiconductor body comprises silicon, silicon germanium, germanium, or gallium arsenide.

22. The transistor of claim 19, wherein the second body portion comprises a channel having a channel length a channel width and a channel depth, and wherein the channel length, the channel width and the channel depth are generally equal.

23. The transistor of claim 19, wherein the second body portion comprises a channel having a channel length of about 25 nm or less.

24. A transistor, comprising:

a formed semiconductor body deposited over a semiconductor starting structure, the formed semiconductor body comprising a first body portion, a second body portion, and a third body portion, the second body portion being disposed over the semiconductor starting material between the first and third body portions and having first and second lateral sides and a top, the first and third body portions individually comprising doped source/drains; and

a gate structure disposed along at least a portion of one or more of the top and sides of the second body portion, the gate structure comprising a conductive gate electrode and a gate dielectric disposed between the gate electrode and the second body portion.